Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A system comprising:

a ~~component~~processor;

a detector to detect a power management event; and

a controller to transition, in response to the power management event, a first setting of the ~~component~~ processor from a first performance mode to a second performance mode, including to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level, the processor to remain in an active mode during the voltage level transition.

~~the controller to transition the component from a reduced activity state, a core component clock remains active during the reduced activity state, and the controller to change a second setting of the component from a first performance mode to a second performance mode.~~

2. (Canceled)

3. (Canceled)

4. (Currently Amended) The system of claim 1, wherein during the frequency level transition the processor is to be placed in a sleep state and not a deep sleep state~~the reduced activity state includes the sleep state~~.

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5. (Canceled)

6. (Previously Presented) The system of claim 4, wherein the core processor clock remains active during the sleep state.

7. (Previously Presented) The system of claim 4, wherein a system clock input to the processor remains active during the sleep state.

8. (Original) The system of claim 1, wherein the power management event includes a change of the system power source from an internal power source to an external power source.

9. (Currently Amended) The system of claim 1, wherein ~~changing the first setting of the component can~~ the voltage level transition requires 5-500 microseconds.

10. (Currently Amended) The system of claim 1, wherein the frequency level transition ~~changing the second setting of the component~~ requires less than 5 microseconds.

11. (Currently Amended) A system comprising:

a ~~component~~processor;

a detector to detect a power management event;

a controller to transition the ~~component~~processor, in response to the power management event, ~~to a reduced activity state, a core component clock remains active during the reduced activity state~~the transition includes to lower the core processor clock frequency from a first frequency to a second frequency, and to lower the core processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during the voltage level transition.

~~the controller to change a first setting of the component from a first performance mode to a second performance mode,~~

~~the controller to transition a second setting of the component from a first performance mode to a second performance mode~~.

12. (Canceled)

13. (Currently Amended) The system of claim 11, wherein during the frequency level transition the processor to be placed in a sleep state and not a deep sleep state.~~the reduced activity state includes the sleep state.~~

14. (Canceled)

15. (Canceled)

16. (Previously Presented) The system of claims 13, wherein a system clock input to the processor remains active during the sleep state.

17. (Previously Presented) The system of claims 13, wherein the core processor clock remains active during the sleep state.

18. (Original) The system of claim 11, wherein the power management event includes a change of the system power source from an external power source to an internal power source.

19. (Currently Amended) The system of claim 12, wherein the frequency level transition ~~changing the first setting of the component~~ requires less than 5 microseconds.

20. (Currently Amended) The system of claim 11, wherein the voltage level transition requires 50 ~~changing the second setting of the component can requires~~ 500 microseconds.

21. (Currently Amended) A computer-readable medium having stored thereon a set of instructions to translate instructions, the set of instructions, which when executed by a processor, cause the processor to perform a method comprising:

detecting a power management event;

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raising a processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during voltage level transition

then raising the processor clock frequency from a first frequency level to a second frequency level,

~~transitioning a first setting of a component from a first performance mode to a second performance mode in response to the power management event,~~

~~transitioning the component out of a reduced activity state, a core component clock remains active during the reduced activity state, and to change a second setting of the component from a first performance mode to a second performance mode,~~

if the power management event includes the system power source switching from an internal power source to an external power source; and

lowering a core processor clock frequency from a first frequency to a second frequency;

lowering a core processor supply voltage level from a first voltage level to a second voltage level, the processor remaining in an active mode during voltage level transition~~transitioning the controller to the reduced activity state in response to the power management event,~~

~~changing the second setting of the component from the second performance mode to the first performance mode,~~

~~transitioning the component to the reduced activity state, and transitioning the first setting of the component from the second performance mode to the first performance mode~~,

if the power management event includes the system power source switching from an external power source to an internal power source.

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Currently Amended) The computer-readable medium of claim 21, wherein the during frequency level transition the processor is placed in a sleep state and not a deep sleep state~~reduced activity state includes a sleep state~~.

26. (Previously Presented) The computer-readable medium of claim 25, wherein the core processor clock remains active during the sleep state.

27. (Canceled)

28. (Canceled)

29. (Previously Presented) The computer-readable medium of claim 25, wherein a system clock input to the processor remains active during the sleep state.

30. (Canceled)

31. (Previously Presented) An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller, in response to the indication, to raise a processor supply voltage level from a first voltage level to a second voltage level, and then to raise the processor clock frequency from a first frequency level to a second frequency level, the processor to remain in an active mode during the voltage level transition.~~a controller to transition, in response to the indication, transition a power supply voltage level of a component from a first level to a second, higher level,~~

~~the controller to transition the component from a low activity state, a core component clock remains active during the low activity state, and to change a core component clock frequency from a first level to a second, higher level, while the component is in the low activity state~~.

32. (Original) The apparatus of claim 31, wherein during the frequency level transition the processor to be placed in a sleep state and not a deep sleep state, and core component clock and a system clock input to the ~~component~~ processor remain active during the ~~low activity state~~sleep state.

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33. (Original) The apparatus of claim 31, wherein the indication is generated in response to a change in a power source in the system from an internal power source to an external power source.

34. (Previously Presented) An apparatus comprising:

a detector to receive an indication to change power states in the system; and

a controller, in response to the indication, to lower a core processor clock frequency from a first frequency to a second frequency, and to lower a core processor supply voltage level from a first voltage level to a second voltage level, the processor to remain in an active mode during the voltage level transition.~~a controller to transition the component to a low activity state in response to the indication, a core component clock remains active during the low activity state,~~

~~the controller to change the component core clock frequency from a first level to a second, lower level, and to transition a power supply voltage level of the component from a first level to a second, lower level~~.

35. (Original) The apparatus of claim 34, wherein during the frequency level transition the processor to be placed in a sleep state and not a deep sleep state, and the core component clock and a system clock input to the component remain active during the ~~low activity~~sleep state.

36. (Original) The apparatus of claim 34, wherein the indication is generated in response to a change in a power source in the system from an external power source to an internal power source.